Appl. No.: 09/871,452
Amdt. dated 03/10/2005
Reply to Office action of 12/10/2004

REMARKS

Applicant wishes to thank the Examiner for consideration of the previous Amendment and for withdrawal of the previously pending 102(e) rejection. All of Claims 1 through 8 are rejected as failing to comply with the definiteness and enablement requirements. Claims 1 through 4 are rejected as identically disclosed in Jamal et al. U.S. Patent No. 5,930,366.

Concerning indefiniteness, the Office Action objects to the phrase "after spread spectrum and scrambling" recited in Claim 1. In order to clarify the recitation of "after spread spectrum and scrambling", Claim 1 has been amended to recite "each time slot is packed with m pre-selected pilot symbols that have been spread spectrum and scrambled." No new matter has been added.

"Spread spectrum and scrambling" refers to spreading and scrambling the pilot symbols but not each time slot. So an attributive clause "that have been spread spectrum and scrambled" is used to modify the pilot symbols.

Concerning enablement, spread spectrum and scrambling are not special operations, and are well known to those of skill in the art, such as spreading and scrambling for dedicated channels and common channels disclosed in the figure 7 of the Jamal reference, or defined in the chart of downlink spreading and modulation of third generation project protocol (3GPP). How to spread and scramble, as defined in the well-known 3GPP specification, is descried in brief as follows in order to illustrate spread and scramble operation:

Figure A illustrates the spreading operation for all downlink physical channels except SCH. Each pair of two consecutive symbols is first serial-to-parallel converted and mapped to an I and Q branch. The mapping is such that even and odd numbered symbols are mapped to the I and Q branch respectively. The I and Q branches are then both spread to the chip rate by the same real-valued channelization code $C_{ch,SF,m}$. The sequences of real-valued chips on the I and Q branch are then treated as a single complex-valued sequence of chips. This sequence of chips is scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$.

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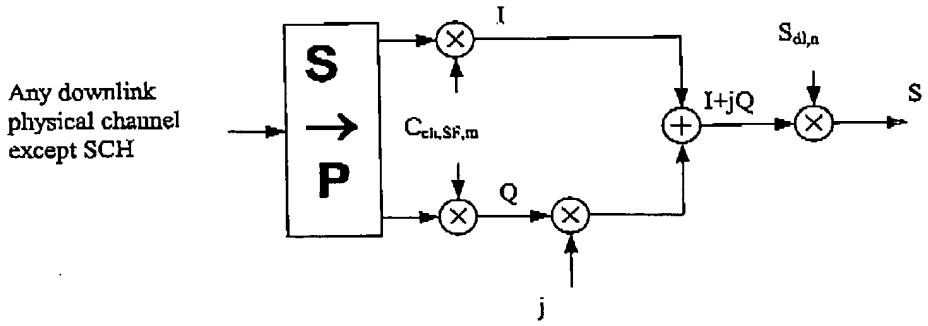

Figure. A

The channelization codes of figure A are Orthogonal Variable Spreading Factor (OVSF) codes that preserve the orthogonality between downlink channels of different rates and spreading factors. The generation method for the channelisation code is defined as:

$$C_{ch,1,0} = 1,$$

$$\begin{bmatrix} C_{ch,2,0} \\ C_{ch,2,1} \end{bmatrix} = \begin{bmatrix} C_{ch,1,0} & C_{ch,1,0} \\ C_{ch,1,0} & -C_{ch,1,0} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

$$\begin{bmatrix} C_{ch,2(n+1),0} \\ C_{ch,2(n+1),1} \\ C_{ch,2(n+1),2} \\ C_{ch,2(n+1),3} \\ \vdots \\ C_{ch,2(n+1),2(n+1)-2} \\ C_{ch,2(n+1),2(n+1)-1} \end{bmatrix} = \begin{bmatrix} C_{ch,2^n,0} & C_{ch,2^n,0} \\ C_{ch,2^n,0} & -C_{ch,2^n,0} \\ C_{ch,2^n,1} & C_{ch,2^n,1} \\ C_{ch,2^n,1} & -C_{ch,2^n,1} \\ \vdots & \vdots \\ C_{ch,2^n,2^n-1} & C_{ch,2^n,2^n-1} \\ C_{ch,2^n,2^n-1} & -C_{ch,2^n,2^n-1} \end{bmatrix}$$

A total of $2^{18}-1 = 262,143$ scrambling codes, numbered 0...262,142 can be generated. However not all the scrambling codes are used. The scrambling codes are divided into 512 sets each of a primary scrambling code and 15 secondary scrambling codes. The primary scrambling codes consist of scrambling codes n=16*i where i=0...511. The i:th set of secondary scrambling codes consists of scrambling codes 16*i+k, where k=1...15. There is a one-to-one mapping between each primary scrambling code and 15 secondary scrambling codes in a set such that i:th primary scrambling code corresponds to i:th set of secondary scrambling codes. The set of

primary scrambling codes is further divided into 64 scrambling code groups, each consisting of 8 primary scrambling codes. The j:th scrambling code group consists of primary scrambling codes 16*8*j+16*k, where j=0..63 and k=0..7. Each cell is allocated one and only one primary scrambling code. The primary CPICH are always transmitted using the primary scrambling code. The other downlink physical channels can be transmitted with either the primary scrambling code or a secondary scrambling code from the set associated with the primary scrambling code of the cell.

The scrambling code sequences are constructed by combining two real sequences into a complex sequence. Each of the two real sequences are constructed as the position wise modulo 2 sum of 38400 chip segments of two binary *m*-sequences generated by means of two generator polynomials of degree 18. The resulting sequences thus constitute segments of a set of Gold sequences. The scrambling codes are repeated for every 10 ms radio frame. Let x and y be the two sequences respectively. The x sequence is constructed using the primitive (over GF(2)) polynomial $1+X^7+X^{18}$. The y sequence is constructed using the polynomial $1+X^5+X^7+X^{10}+X^{18}$ .The configuration of downlink scrambling code generator is shown in Figure B.

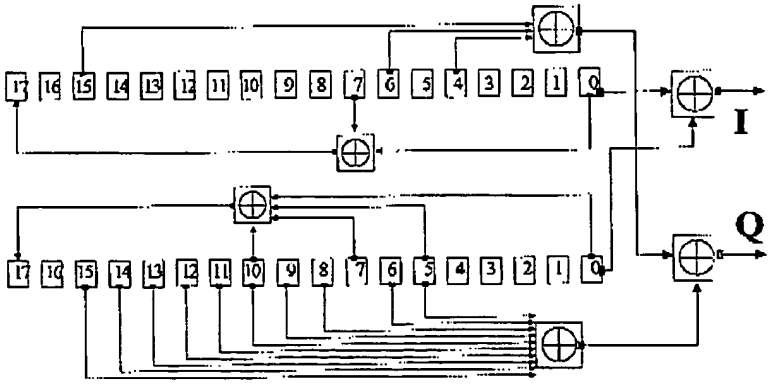

Figure B

Whereas the terminology of Claim 1 has been clarified and shown to be commonly understood in the art, it is respectfully requested that the pending indefiniteness and enablement rejections be removed.

Regarding the rejections in view of prior art, Jamal et al. discloses a pilot synchronization channel structure for a CDMA system, comprising a synchronization channel (SCH) (for example, combined channel in figure 7) and a pilot channel overlapping the SCH (for example, pilot channel in figure 7), wherein the pilot channel comprises data frames comprising p time slots and each time slot is packed with m pre-selected pilot symbols. However, the claimed invention is distinguished from the disclosure of Jamal on several grounds.

Firstly, the claimed synchronization channel is not the combined channel in figure 7 of the Jamal reference. As shown in Claim 1, the synchronization channel is defined in wideband code division multiple access protocol, so it comprises a primary synchronization code (PSC) and a secondary synchronization code (SSC), shown in figure 1 of the application, wherein the primary synchronization code is just the pilot code $\bar{c}_p$ shown in figure 1 to 7 of the Jamal reference, which is used to find downlink chip boundaries, symbol boundaries and frame boundaries of this timing reference clock (column 2, lines 38-47); the secondary synchronization code responds to the combined code $\bar{c}_{s/i,i}$ shown in figures 5 to 7 or to the frame synchronization code $\bar{c}_s$ shown in figure 4 of the Jamal reference. Therefore, the claimed synchronization channel includes the pilot channel shown in figure 7 of the Jamal reference and the combined channel which are shown in figure 7 of the Jamal reference but not only the combined channel.

Secondly, the claimed pilot channel overlapping the SCH of the invention is not the pilot channel (primary synchronization channel) in figure 7 of the Jamal reference. The reason is as follows:

(1) Recited as the specification of the invention, the pilot codes in the pilot channel overlapping the SCH are extra common pilot signals and are used to demodulate data, estimate channel, execute the physical measurement simply and conveniently for cell search, handoff and power control, but the pilot codes in figure 7 of the Jamal reference are the primary synchronization codes and are used to find downlink chip boundaries, symbol boundaries and frame boundaries of this timing reference clock (column 2, lines 38-47);

(2) The pilot codes in the pilot channel overlapping the SCH are spread spectrum and scrambled in order to distinguish cells, but the pilot codes in figure 7 of the Jamal reference are not scrambled (column 6, lines 5-8) because they are the primary synchronization codes for synchronization.

(3) It is obvious that the pilot channel of the invention is overlapped in the SCH that comprises a primary synchronization code (PSC) and a secondary synchronization code, but the pilot channel (primary synchronization channel) in figure 7 of the Jamal reference is overlapped in combined channel (an equivalent to the secondary synchronization channel), namely, primary synchronization channel overlapping the secondary synchronization channel (figure 5-7 of the Jamal reference).

Thirdly, based on the invention, the pilot synchronization channel structure could be shown as figure C:

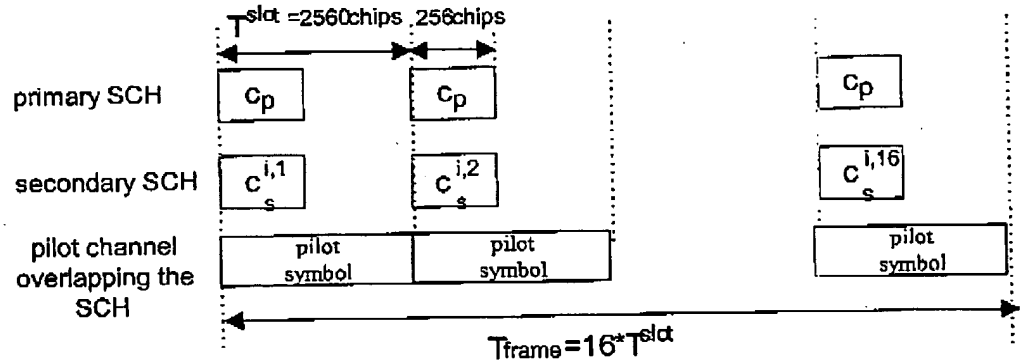

Figure C

In view of the above figure, it is obvious that the pilot channel overlapping the SCH is not disclosed or suggested in the Jamal reference.

Whereas the claimed invention has been shown to be patentably distinct from the cited reference, Applicant respectfully submits that the prior art rejections have been overcome.

In view of the amendments and remarks made above, Applicant submits that the pending claims are now in condition for allowance and an indication of allowability of the claims is solicited.

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It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit Account No. 16-0605.

Respectfully submitted,

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Tamara Stevens

March 10, 2005
Date